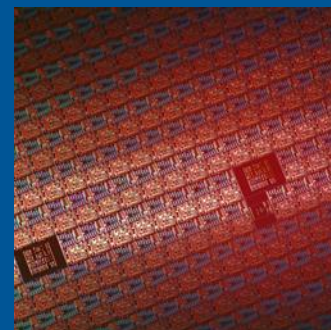




Accelerating the next technology revolution

# EUV Status and Outlook

Stefan Wurm  
Director Lithography  
SEMATECH



# Where is EUV today

## *The birds-eye view*



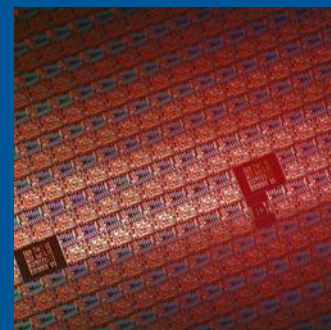
### This presentation's focus

- The good news
  - EUV resists are in good shape for EUV introduction
  - EUV sources are being worked at hard
  - The first production type exposure tools are being delivered
- The challenges near-term (22 – 16 nm half-pitch)
  - Getting EUV source performance up
  - Getting EUV mask blanks ready to support HVM introduction (22 nm half-pitch)
- The challenges long-term (< 16 nm half-pitch)
  - EUV source power scaling
  - Imaging materials performance
  - Developing the infrastructure to enable EUV mask blank / mask technology



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# EUV Resists



# EUV Resist Cycles of Learning

## *Scope*

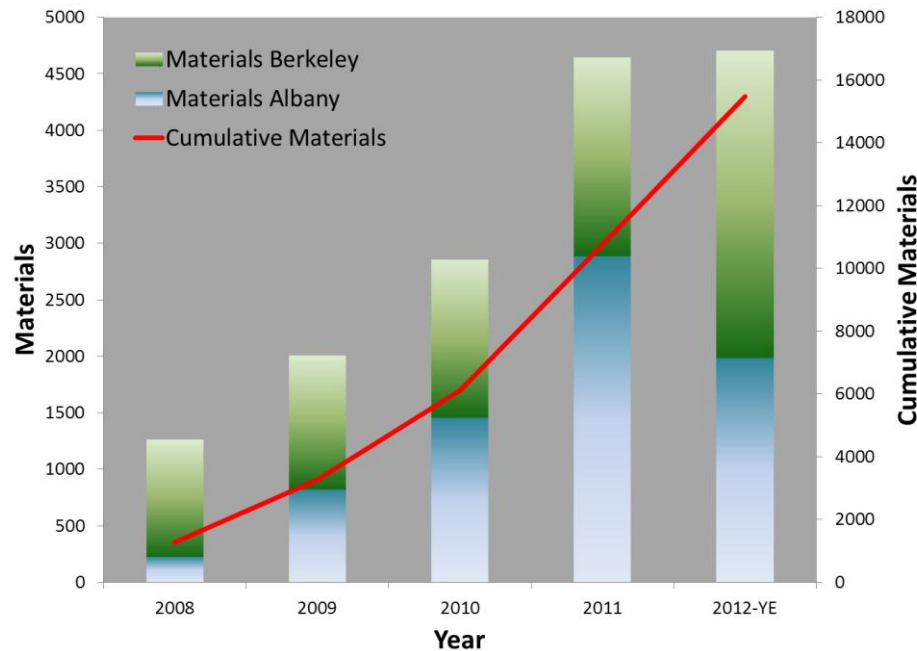


- Use SEMATECH's Microexposure tools (METs) to drive EUV resist material cycles of learning at materials suppliers
- Benchmark the industries progress towards achieving 22/16 nm half-pitch imaging performance

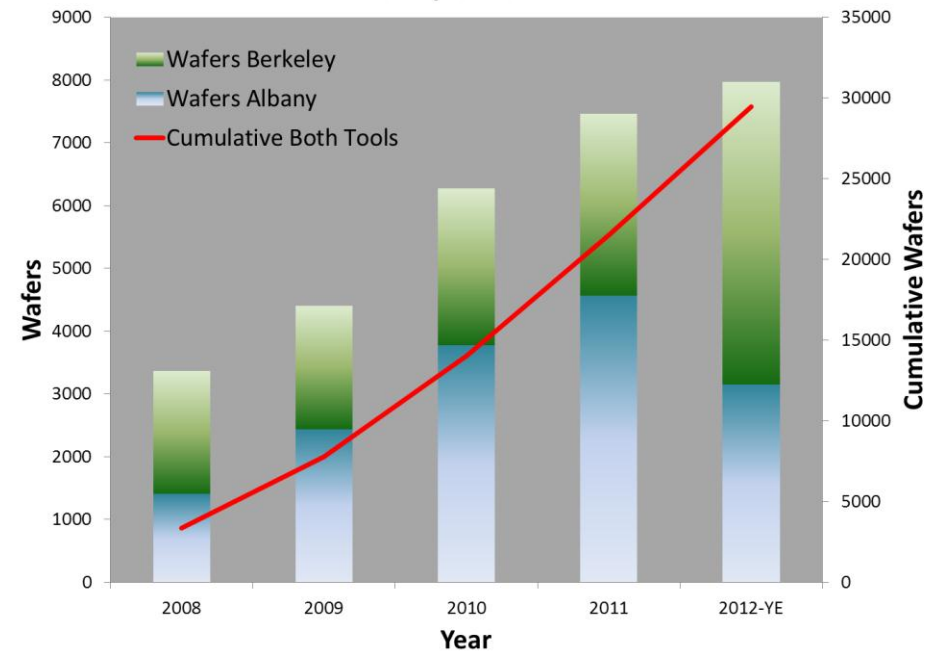
# SEMATECH Resist and Materials Development Center (RMDC)



Materials Processed at RMDC



Wafers Exposed at RMDC



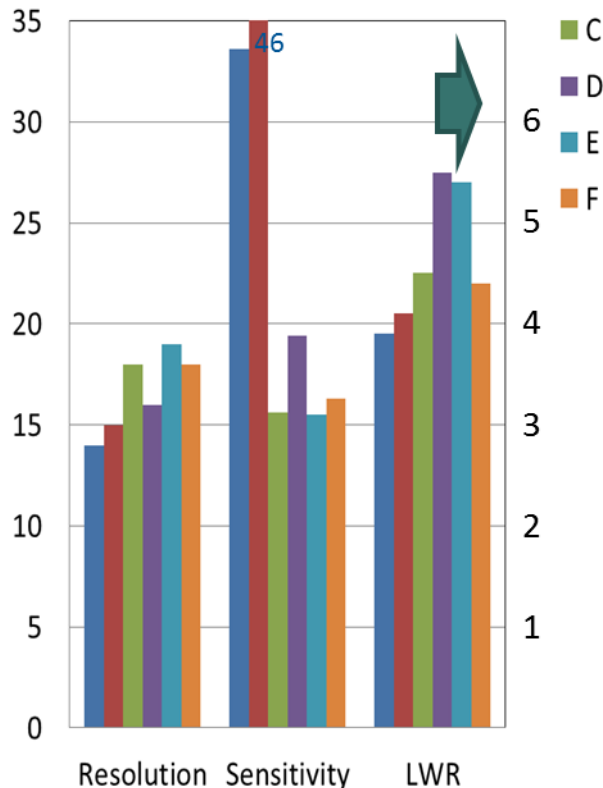
- >15000 materials and >29000 wafers have been processed at RMDC since 2008 (Albany MET & LBNL MET)
- In 2012, 4703 materials (1981 Albany MET, 2722 LBNL MET) and 7972 wafers were processed (3153 Albany MET, 4819 LBNL MET)

# L/S EUV Resist Performance Status

## *Pseudo PSM @ SEMATECH's Tool in Berkeley*



Performance against key metrics



	20nm	19nm	18nm	17nm	16nm	15nm	14nm	13nm
H 33.6mJ	19.3/4.3	18.4/3.5	17.6/3.7	16.4/3.9	15.1/3.7	14.7/3.7	12.5/3.8	
I 46.0mJ	15.3nm/3.9nm	16.1nm/4.2nm	15.8nm/4.3nm	14.5nm/4.0nm	13.1nm/3.6nm	11.6nm/4.2nm	11.3nm/4.5nm	
J 15.6mJ	19.2nm/4.8nm	18.5nm/4.3nm	17.7nm/4.4nm					
K 19.4mJ	19.2/6.2	17.8/4.9	17.2/4.1	15.6/4.9	14.7/4.7			
L 15.5mJ	20.7/4.8	19.6/6.0						
M 15.4mJ	21.1nm/4.2nm	19.9nm/4.5nm	18.3nm/4.8nm					



Best resist for each supplier

- Berkeley MET, PPSM
- 30nm Resist THK



# Recent Contact Hole Results

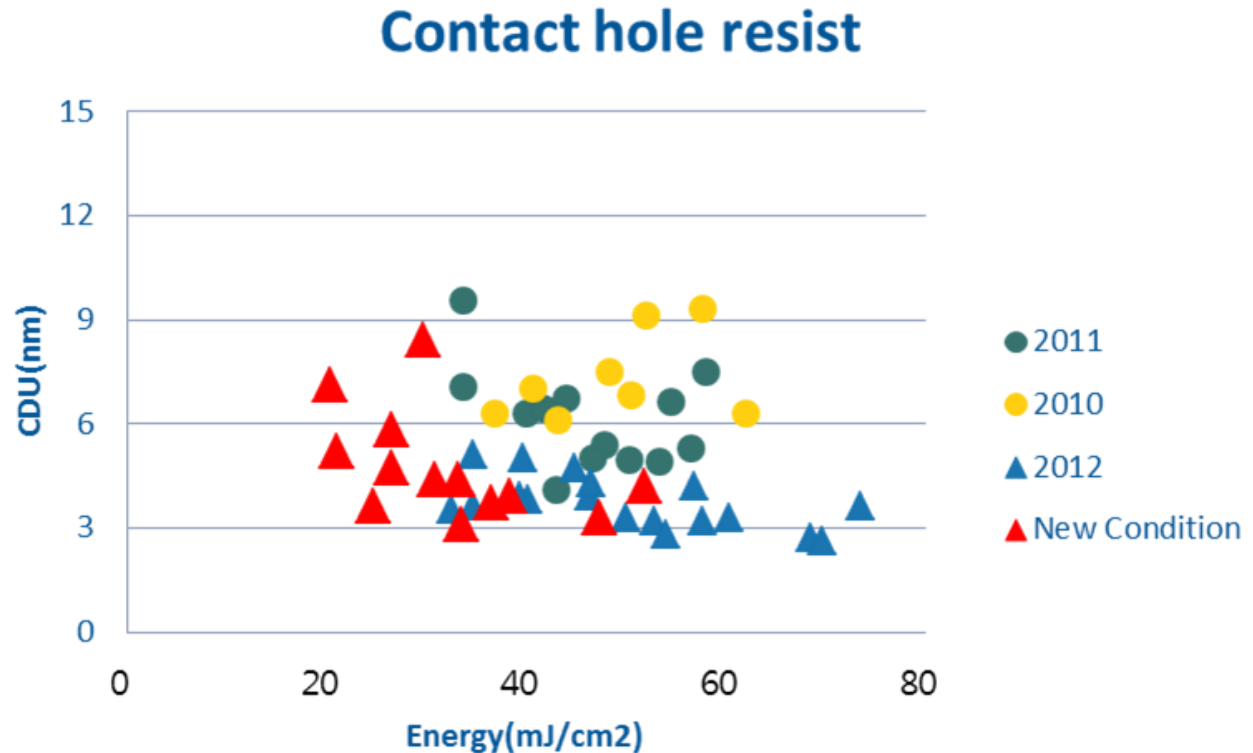


- 2010 – 2012 condition:

- Annular
- 30 nm HP
- 0% bias
- 80 nm FT,

- New condition:

- Quad
- 26 nm HP
- 20% bias
- 60 nm FT



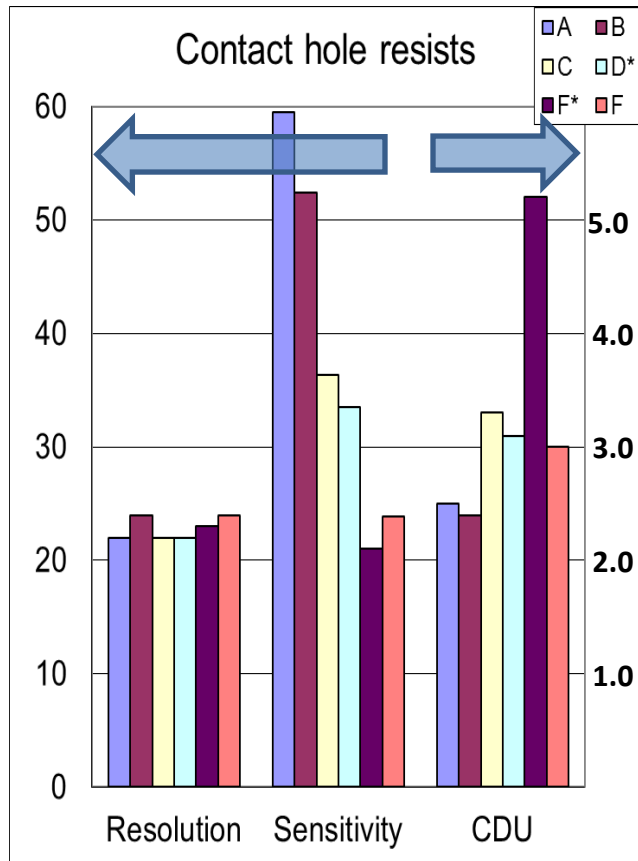
- Leading edge  $3\sigma$  CDU of 3 nm or less can now be achieved at less than 40 mJ/cm<sup>2</sup> with zero mask bias
- Improved exposure conditions show leading edge CDU at less than 30 mJ/cm<sup>2</sup>

# C/H EUV Resist Performance Status



Berkeley MET: Quad, NA 0.3, sigma 0.48~0.68  
 FT 80nm (A,B,C,F); 60nm; D, E  
 No mask bias (A,B,C,F) (+20% Bias)

D\*, E\*: 60 nm FT & +20% bias



\* CDU was measured at 26nm HP

	26nm	24nm	23nm	22nm	21nm	20nm
A						59.5mJ/cm2 2.5nm
B						52.4mJ/cm2 2.4nm
C						36.3mJ/cm2 3.3nm
D*	 25nmHP					33.5mJ/cm2 3.1nm
E*	 25nmHP					21.0mJ/cm2 5.2nm
F						23.9mJ/cm2 3.0nm

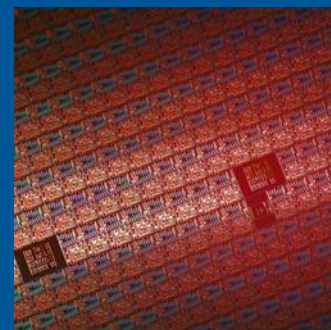


- Work to improve existing resist platform continues full speed
  - Resolution, LWR and CDU are getting better but only by accepting slower resists
- The industry needs to increase research efforts in alternative approaches so we will have materials that can support < 11 nm half-pitch nodes
  - Nanoparticle materials
  - Negative tone materials
  - Metallo-organic resist materials
  - etc...



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# EUV Mask Blanks



# EUV HVM Mask Blanks

## *Key Challenges*



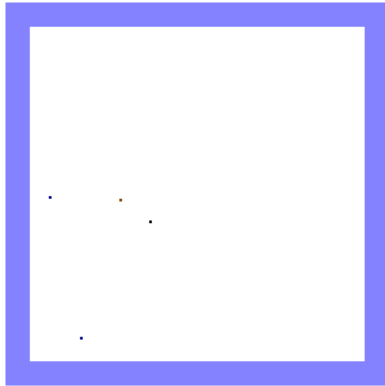
- Mask Defect Density
  - Mask Blank Defects > 100nm\*
    - Yield of useable mask blanks and patterned masks
  - Mask Blank Defects < 100nm\*
    - Limited defect counts needed to enable mitigation schemes
  - Mitigation strategies
    - Feature level OPC
    - Pattern shift
    - Defect Repair
    - etc...
  - Adder Defects
    - The entire EUV mask ecosystem needs improvements to manage working with pellicle free reticles

\* SiO<sub>2</sub> equivalent

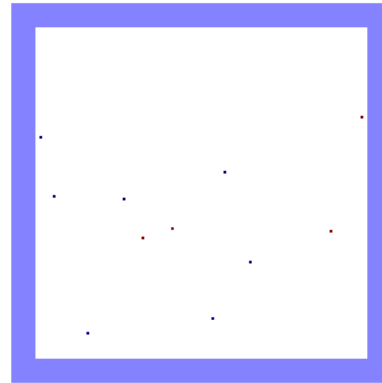
# SEMATECH Champion Data



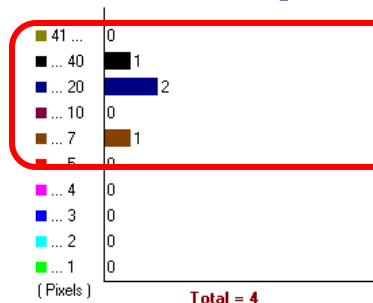
M1350



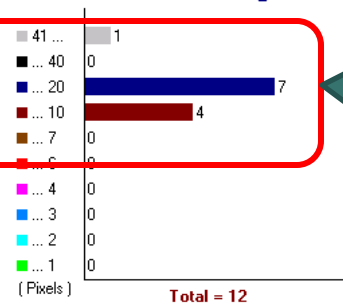
M7360 Dense Scan



Pixel Histogram



Pixel Histogram



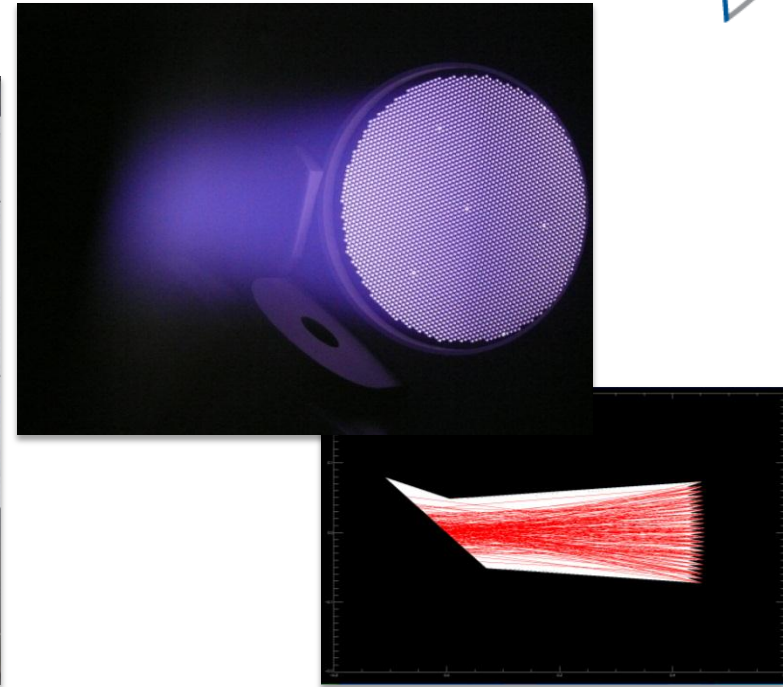
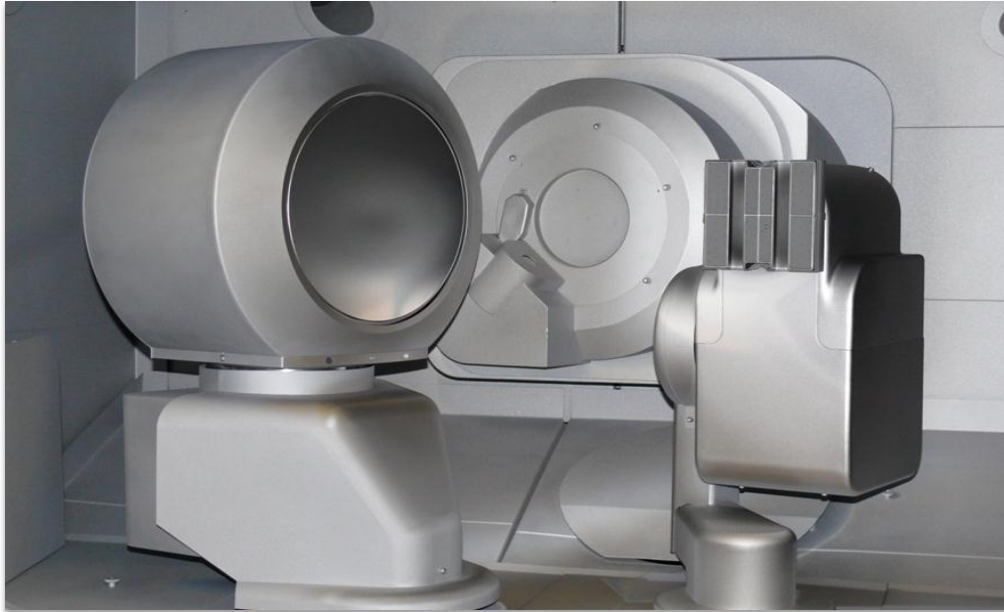
- Large defects – would not be considered a useable HVM mask blank
- Large defects are from deposition
- Elimination of large defects is current focus of SEMATECH's mask program

- Achieved 12 defects @45nm\* or 8 defects @50nm\* from M7360 inspection
  - 10 pits (from substrate), 1 handling defect, 1 defect from deposition

\* SiO<sub>2</sub> equivalent

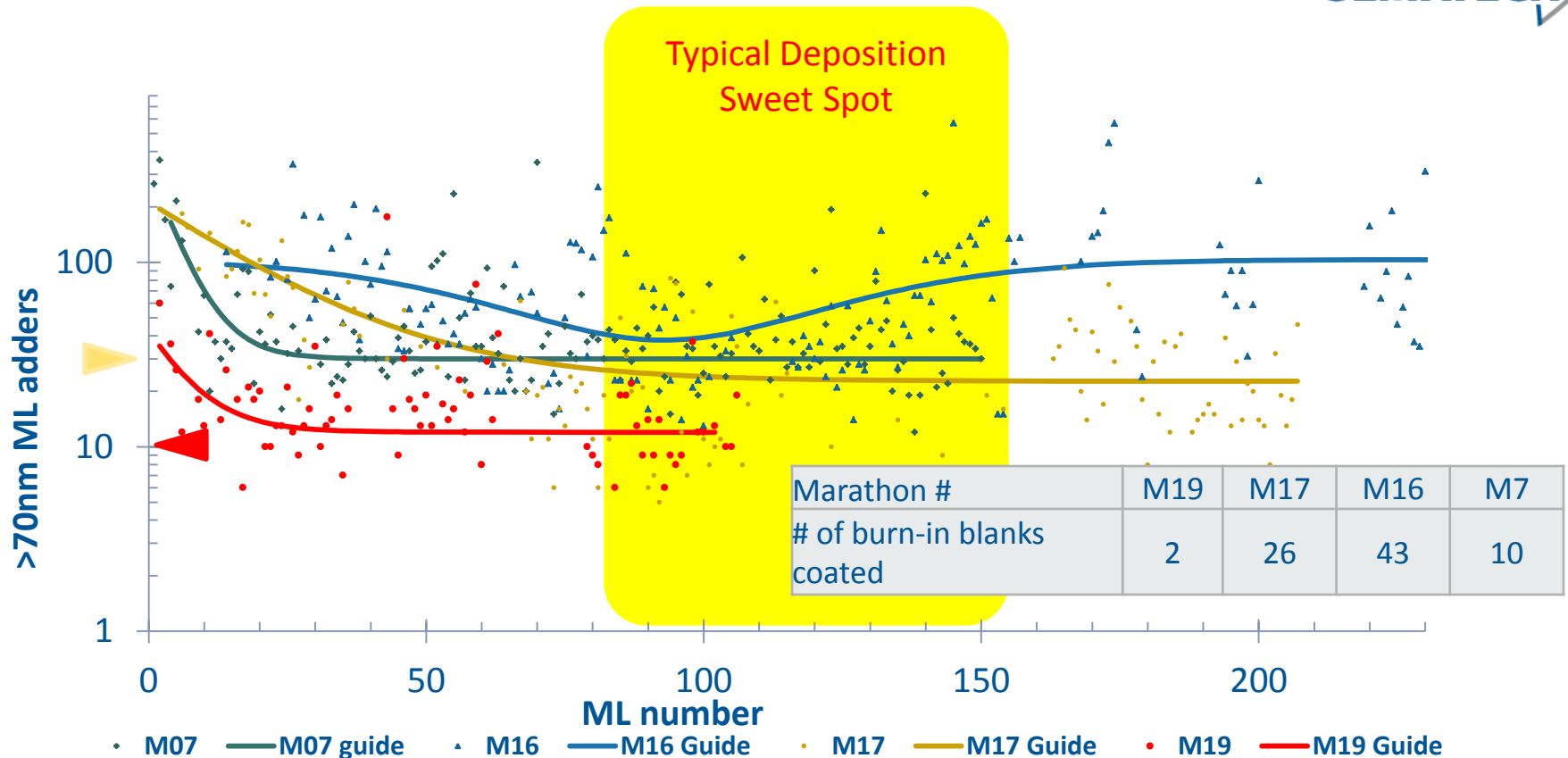
# Mask Blank ML Deposition

## *Veeco Nexus IBD Tool*



- Ion Beam Deposition (IBD)
  - The leading technology for deposition of mask blank Si/Mo multilayers
  - Has demonstrated potential to achieve useable EUV mask blanks
    - But high variability in handling defects and deposition excursions have limited further isolation of deposition defect sources

# Current Deposition Results



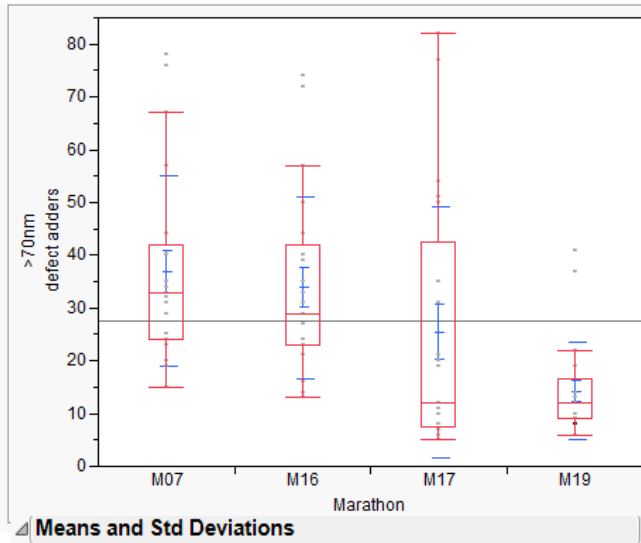
- Results of recent process changes introduced by SEMATECH
  - Reduction in deposition defect adders (@70nm\*) to consistent single digit performance
  - Less variability in deposition defect counts
- Allowing for 10 defect adders the yield of the most recent marathon deposition run is 2.5X better than the previous best marathon

\* SiO<sub>2</sub> equivalent



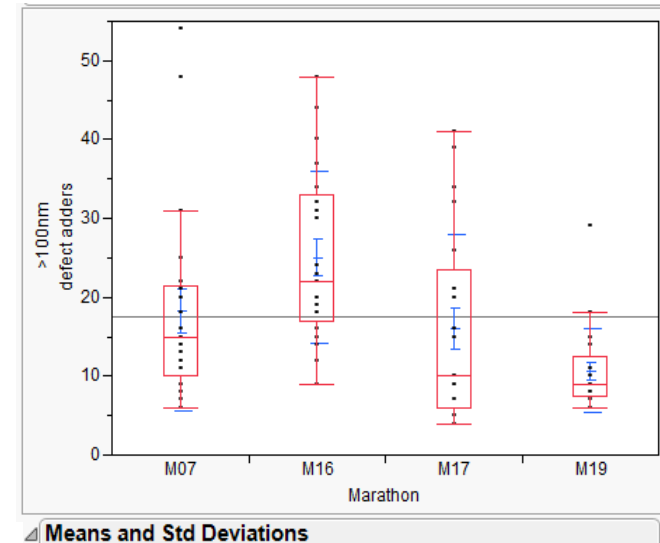
# Variability of Defect Counts

>70nm\* adders



Level	Number	Mean	Std Dev	Std Err		
				Mean	Lower 95%	Upper 95%
M07	21	36.9048	18.0303	3.9345	28.697	45.112
M16	21	33.8571	17.3098	3.7773	25.978	41.736
M17	21	25.4286	23.8172	5.1973	14.587	36.270
M19	21	14.2381	9.2785	2.0247	10.015	18.462

>100nm\* adders



Level	Number	Mean	Std Dev	Std Err		
				Mean	Lower 95%	Upper 95%
M07	21	18.2857	12.6576	2.7621	12.524	24.047
M16	21	25.0476	10.8925	2.3769	20.089	30.006
M17	21	15.9524	11.9561	2.6090	10.510	21.395
M19	21	10.6667	5.3135	1.1595	8.248	13.085

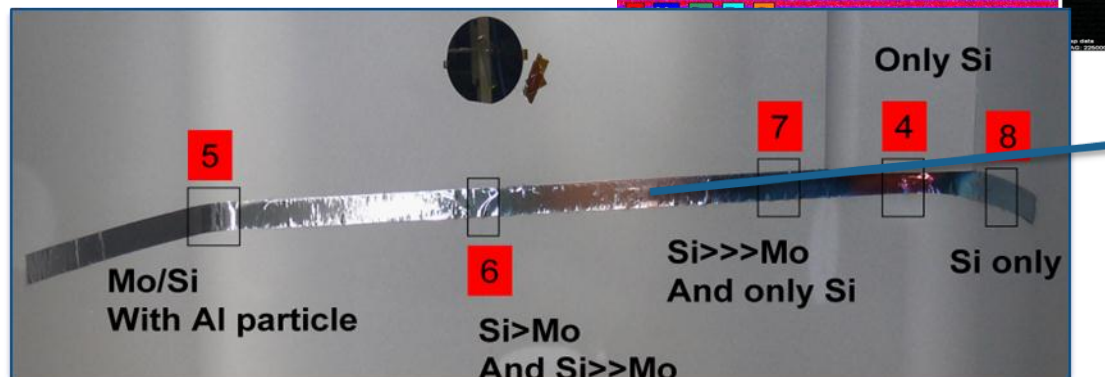
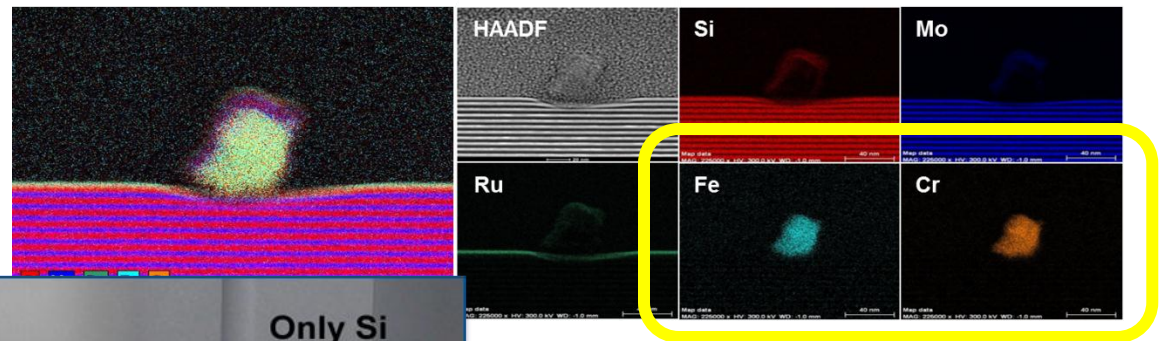
- Current deposition run is performing with greater consistency and at lower defect levels
  - Improvement @ 70nm\* in mean and 3-sigma
  - Range between upper and lower 95% is narrower
  - Repeatable defect signature between mask blanks
- Major step towards validating that IBD can support HVM manufacturing of EUV mask blanks

\* SiO<sub>2</sub> equivalent

# Source of Large Defects

## *Defects sputtered from IBD chamber shields*

- According to the early ion source modeling virtually all of the ion beam should hit the target
- Many mask blank defects added during the ML deposition process look chemically like shield material
  - Testing indicates that the majority of these defects are liberated by the ion beam missing the target and hitting the shields
  - Understanding why the ion beam miss the sputtering targets is crucial to reducing defects



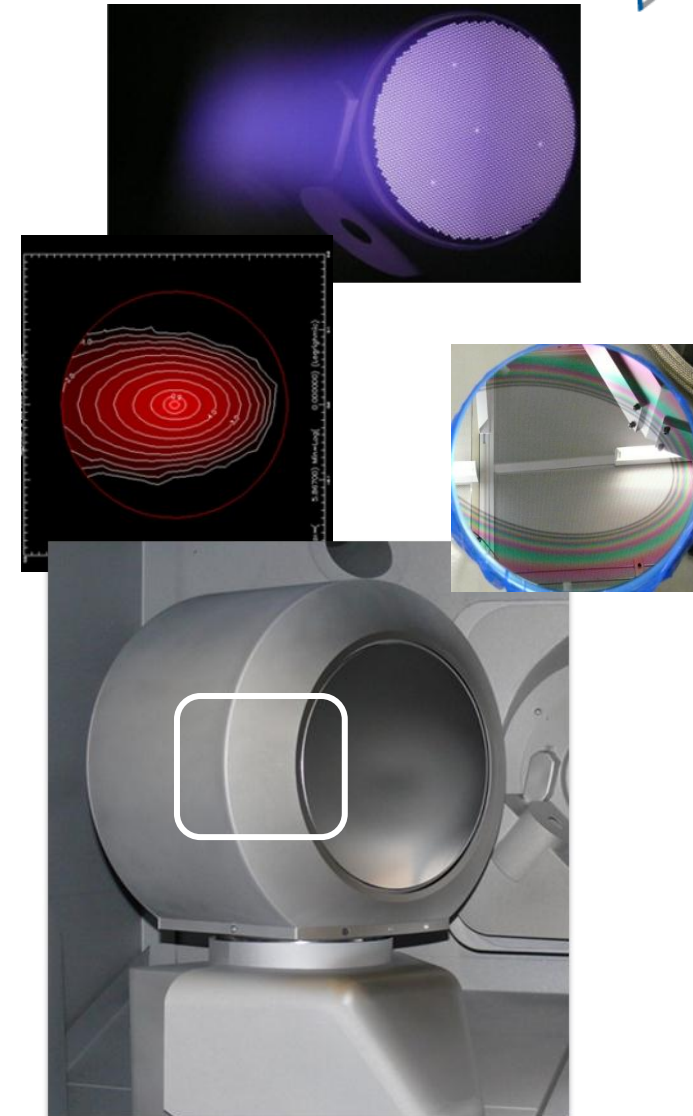
**Area of net etch on shield**

# Improvement of Deposition

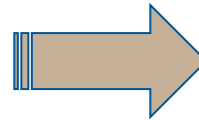
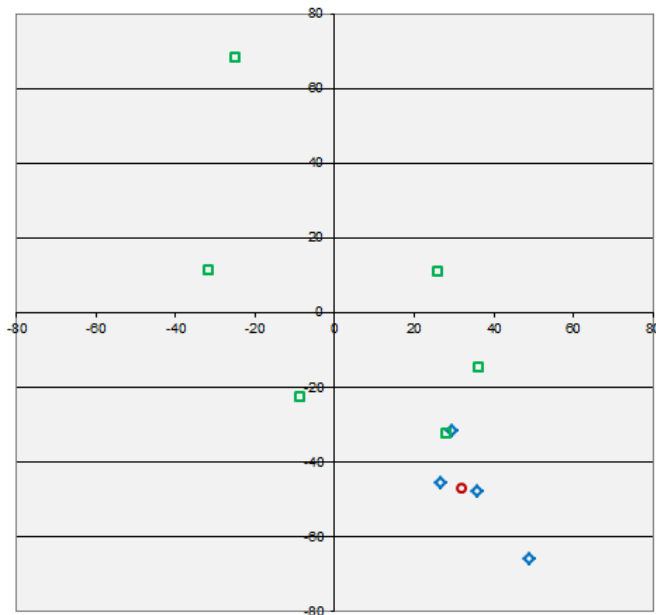
## *Ion Source Containment*



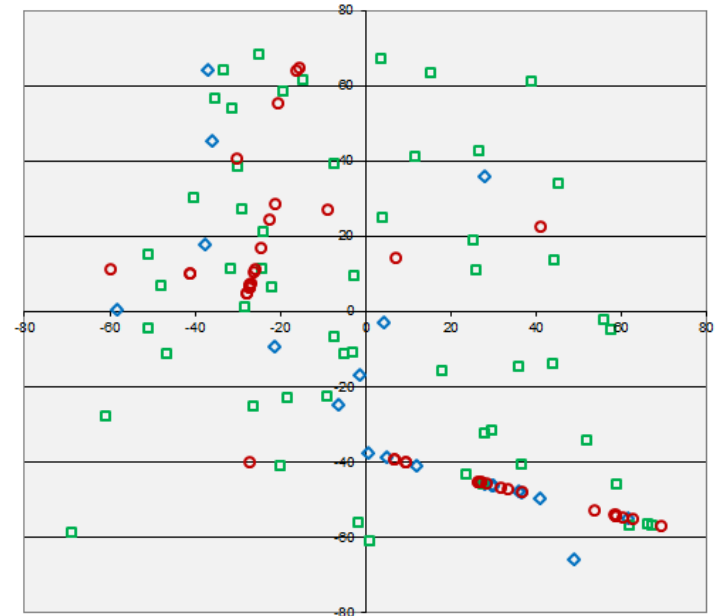
- The IBD ion beam has a significant overspill
  - Causing significant etching of
    - Edges of target
    - Shields near target
    - Door Shields and nearby areas
  - Source of the large size defects originating from the shields
- SEMATECH's current objective is to work with the tool supplier to improve ion source confinement
  - Test new ion source operation parameters and high chamber pumping speeds
  - Objective is to reduce overspill and scattering



# Limitation in Detection



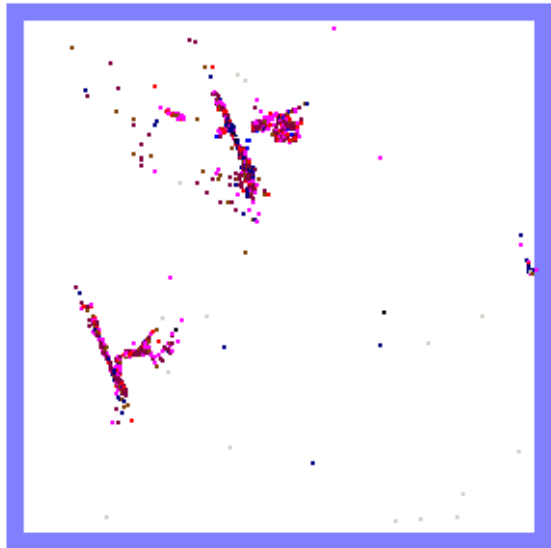
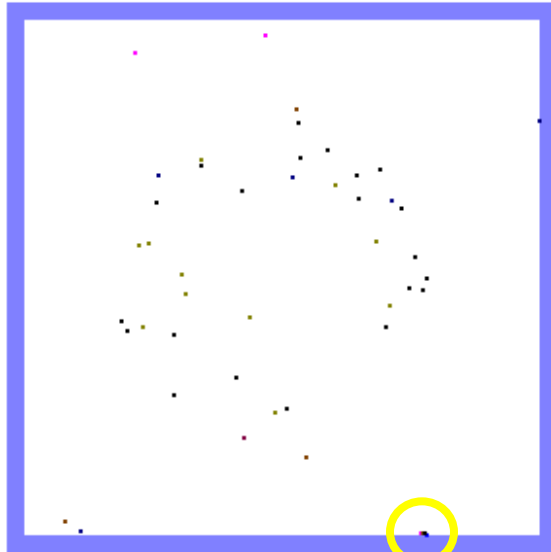
**Deposition**



Defectivity	Pits	Scratches	Particles	Pit+Scr
Substrate @ 40 nm SiO <sub>2</sub> size	5	2	4	7
ML blank @ 43 nm SiO <sub>2</sub> size	56	43	21	99

- Majority of the small sized pits, bumps and scratches do not show up until after decoration by the multilayer deposition
- Current substrate inspection capability not able to detect these defects
  - This gap is not being adequately addressed by the industry

# Incoming Material to IBD



- Current issues
  - Handling
    - Edge scratches from handling
    - Excursions with a new handling cassette design
  - Organic contamination
    - Induced by substrate defect inspection
- Overall substrate quality
  - Greatly improved
  - Still a significant contributor to total defects

# Near-future Mask Blank Challenges



- IDMs are using pre-production exposure tools
  - Mask lifetime is becoming a significant problem
    - Keeping the exposure surface of an EUV mask clean and particle free
    - Pattern and reflectance degradation due to repetitive cleaning
    - Damage to the CrN backside
  - Potential mitigation schemes
    - Pellicles
    - Changes in the ML film stack or capping layer to address cleaning damage
    - Possible move to a different backside coating
- Ability of high energy IBD to support future mask blank requirements
  - As defect size specifications will get further constrained
  - Sputtering and scattering of unwanted material will become much harder to control
  - SEMATECH is evaluating a low-energy IBD approach
    - Has some advantages over current process
    - Reflectance uniformity and defect performance still need to be validated



# Key Takeaways

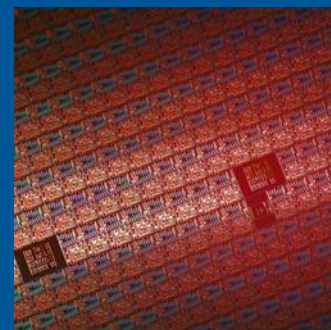


- Current assumption is that IBD can produce useable HVM mask blanks
  - Needs to reach a defect level where mitigation is possible
  - Every indication points to this being possible for the near term
    - Greatly improved process variability
    - Consistent mask blank defect signature
  - Still needs to be validated
  - Long term viability of a high energy IBD process is being questioned
- Substrate Quality
  - Surface defects and finishing continue to improve
  - Continuous improvement significantly hampered by lack of defect metrology
- In-fab Use of EUV Mask and Mask Lifetime
  - Need to ensure that adders are not patterned
    - Move to pellicles
  - Mask lifetime – learning has just begun but already issues seen
    - Backside coating damage
    - Clean handling
    - Pattern mask cleaning



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# Summary



# EUV Lithography Outlook



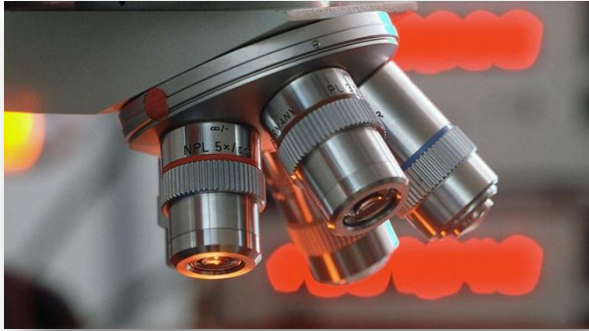
- Scanner/source must meet productivity requirements for EUV to be the cost effective solution
  - This is a pre-condition for EUV to make it into HVM. The industry is investing the resources required to successfully meet this challenge.
  - With the first production type tools in field, the next 12 months will need to demonstrate scanner/source readiness to support EUV HVM ramp-up
- EUV resist are ready to support EUV HVM introduction
  - We are now looking at “realistic” resist sensitivities so to meet productivity requirements the source will need to do more
- EUV mask blank supply chain is the weak link for EUV HVM introduction
  - The source may well be meeting expectations in the next 12 months but without additional investments, EUV mask blanks will not be available at the quality and volume needed for EUV HVM ramp-up
  - The industry needs to strengthen the mask blank supply chain – tools, materials, processes – to enable EUV HVM ramp-up

# Acknowledgement



- Frank Goodwin, SEMATECH
- Mark Neisser, SEMATECH
- Dominic Ashworth, SEMATECH

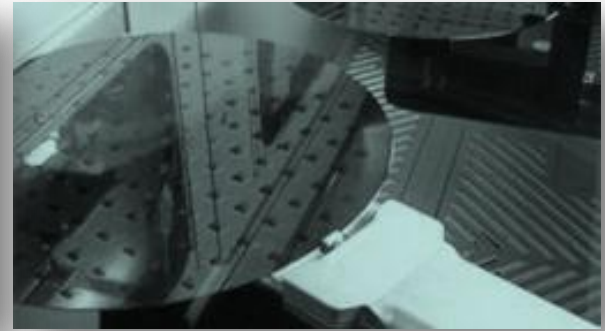
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Research



Development



Manufacturing

# Thank You